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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/008,968	12/06/2001	Ray Mentzer	10010675-1	3781

7590 10/18/2005

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EXAMINER	
JELINEK, BRIAN J	

ART UNIT	PAPER NUMBER
2615	

DATE MAILED: 10/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/008,968	MENTZER, RAY	
	Examiner	Art Unit	
	Brian Jelinek	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *17-20* is/are allowed.

6)☒ Claim(s) *1-3,6-11 and 13-16* is/are rejected.

7)☒ Claim(s) *4,5 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendment

The Examiner respectfully submits a response to the amendment received on 8/11/2005 of application no. 10/008,968 filed on 12/6/2001 in which claims 1-20 are currently pending.

Arguments

The Applicant argues that Fossum does not teach or suggest both an output node and a common node, but rather that the pixel circuit includes a single node for outputting signals (i.e., the node located between transistors 60 and 65).

In response, the Examiner notes that Fossum clearly shows two nodes, wherein the node located between transistors 60 and 65 is connected to the input node of the CDS circuit (Fig. 3A, element 70, node between SHS and SHR transistors; Fig. 3B, column line) via a signal line.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 6-11, and 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fossum et al. (U.S. Pat. No. 5,949,483).

Regarding all claims, Fossum discloses a multiresolution imaging array, wherein the photosensitive element comprises either a photogate or a photodiode (Abstract). Fossum further discloses (Fig. 3) that the array comprises pixels, wherein a pixel comprises a photosensitive element and associated circuitry (30-50) and row decoder elements (55, 60). Fossum further discloses a readout circuit comprises a load transistor 65 and a correlated double sampling circuit 70, wherein the load transistor 65 and correlated double sampling circuit 70 are deleted from the individual pixel cells and are located at the bottom of each column of the array (Fig. 3B) in order to maximize photosensitive cell area. Fossum further discloses one embodiment of a multiresolution imaging array using the common load transistor 65 and sampling circuit 70 arrangement of Fig. 3B (col. 11, lines 3-40), wherein a column average sensor 608 and a row average circuit averages blocks of pixels (Fig. 7, elements 608 and 610), provides varying image resolution image data in order to eliminate unnecessary processing steps associated with obtaining a more detailed image (col. 4, lines 10-39; col. 10, lines 12-53). Fossum further discloses an alternative embodiment of the multiresolution imaging array, wherein contiguous photosensitive elements are interconnected in blocks and the average block values are outputted (col. 4, lines 43-55; col. 17, line 65-col. 18, line 42).

Regarding claim 1, Fossum discloses an optical sensor array (Fig. 7, element 602) comprising: an array of pixel circuits (Fig. 3B, element 15; Fig. 3A, elements 30-60), each pixel circuit including a photo detector (Fig. 3A, element PG) and a voltage supply line (Fig. 3A, VDD of source follower transistor 55), and an output node (Fig. 3A, pixel output between row transistor 60 and load transistor 65) for outputting image

signals from the pixel circuit, wherein the voltage supply line of each pixel circuit is connected to a common node (Fig. 3A, 70 and Fig. 3B, 70; Fig. 3B, column lines) separate from the output node because it is clear from Figs. 3A and 3B that the output node and common node are connected by a signal line; a voltage supply input (Fig. 3A, VDD of source follower transistor 55) configured to be coupled to a voltage supply (Fig. 3A, VDD of source follower transistor 55) and to the common node for supplying a voltage to each pixel circuit; and a sensing circuit coupled to the common node for sensing signals at the common node (Fig. 3B, element 70; Fig. 3A, element 70) and outputting at least one signal representative of an average intensity of light directed onto the array of pixel circuits (col. 17, line 66-col. 18, line 42).

Regarding claim 2, Fossum discloses a switching device coupled between the voltage supply input and the common node for selectively connecting and disconnecting the voltage supply input and the common node (Fig. 3A, element 60).

Regarding claim 3, Fossum discloses the switching device is a transistor (Fig. 3A, element 60).

Regarding claim 6, Fossum discloses the at least one signal output by the sensing circuit includes a reference signal (Fig. 3A, V Out R) and an integration signal (Fig. 3A, V Out S), the optical sensor array further comprising: a column amplifier coupled to the sensing circuit for receiving the reference signal and the integration signal, the column amplifier configured to output a difference signal representing a difference between the reference signal and the integration signal (Fig. 3A, differential amplifier between V Out S and V Out R).

Regarding claim 7, Fossum discloses a gain amplifier coupled to the column amplifier for receiving the difference signal from the column amplifier and outputting an amplified difference signal (Fig. 3A, differential amplifier between V Out S and V Out R).

Regarding claim 8, Fossum discloses the average block value is output by a conventional multiplexer, such that the pixel cell values are read (Fig. 3B, element 21; Fig. 7, element 610). Fossum does not disclose an analog-to-digital converter coupled to the gain amplifier for receiving and digitizing the amplified difference signal, and outputting at least one digital value. Official Notice is given that it is extremely well known in the art to provide an ADC to digitize the analog values provided by the photosensitive elements in an imaging array in order to perform subsequent image processing. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to have provided an ADC to digitize the analog values provided by the photosensitive elements in an imaging array in order to perform subsequent image processing.

Regarding claim 9, please see the rejection of claim 8. Fossum further teaches outputting camera exposure information because pixel values, broadly interpreted, comprise exposure information.

Regarding claim 10, Fossum discloses a digital controller configured to output control signals for controlling operation of the pixel circuits and the sensing circuit (Fig. 3B, elements 18 and 19).

Regarding claim 11, Fossum discloses the digital controller comprises: a register set for providing selectable modes of operation of the optical sensor array, the modes of

operation including at least one normal mode of operation (normal/full resolution mode) and a global (multi-resolution/low resolution) mode of operation (col. 17, line 66-col. 18, line 42). Furthermore, Fossum teaches a timing controller coupled to the register set for generating the control signals based on a selected mode of operation because it is implicit to provide a timing controller to generate control signals in order to correctly perform readout according to a desired mode operation.

Regarding claim 13, please see the Examiner's note regarding all claims supra. Fossum further discloses a method of obtaining average scene intensity information from a pixel array (col. 4, lines 10-55), the pixel array including a plurality of pixel circuits (Fig. 3B, element 15; Fig. 3A, elements 30-60), each pixel circuit coupled to a common node (Fig. 3A, 70 and Fig. 3B, 70, output of CDS circuit; Fig. 3B, column lines) that is configured to be coupled to a voltage supply (Fig. 3A, VDD of source follower transistor 55), each pixel circuit including an output node for outputting image signals from the pixel circuit Fig. 3A, pixel output between row transistor 60 and load transistor 65), the method comprising: isolating the pixel circuits from the voltage supply (Fig. 3A, element 60) because the transistor selectively connects, i.e. isolates, the voltage supply from the pixel output; sensing signals at the common node generated by the plurality of pixel circuits (Fig. 3B, element 70; Fig. 3A, element 70); and generating at least one signal based on the sensed signals, the at least one signal representative of an average intensity of light directed onto the pixel array (col. 17, line 66-col. 18, line 42).

Regarding claim 14, Fossum discloses the at least one signal includes a reference signal (Fig. 3A, V Out R) and an integration signal (Fig. 3A, V Out S), the

method further comprising: generating a difference signal representing a difference between the reference signal and the integration signal (Fig. 3A, differential amplifier between V Out S and V Out R).

Regarding claim 15, Fossum discloses the average block value is output by a conventional multiplexer, such that the pixel cell values are read (Fig. 3B, element 21; Fig. 7, element 610). Fossum does not disclose generating at least one digital value based on the difference signal. Official Notice is given that it is extremely well known in the art to provide an ADC to digitize the analog values provided by the photosensitive elements in an imaging array in order to perform subsequent image processing. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to have provided an ADC to digitize the analog values provided by the photosensitive elements in an imaging array in order to perform subsequent image processing.

Regarding claim 16, please see the rejection of claim 15. Fossum further teaches outputting camera exposure information because pixel values, broadly interpreted, comprise exposure information.

Allowable Subject Matter

Claims 4-5, 12, and 17-20 are allowable or would be allowable if rewritten to overcome any and all objections.

Regarding claim 4, the reason for allowance is as follows: the prior art does not disclose or fairly suggest a sensing circuit wherein the third transistor is coupled

between the voltage supply input and the second current source in combination with all other elements in the claim.

Regarding claim 12, the reason for allowance is as follows: the prior art does not disclose or fairly suggest the control signals generated by the timing controller during the global mode of operation include causing the pixel circuits to be isolated from the voltage input in combination with all other elements of the claim.

Regarding claim 17, the reason for allowance is as follows: the prior art does not disclose or fairly suggest a circuit for obtaining average scene intensity information from a pixel array having a plurality of pixel circuits, each pixel circuit coupled to a common power supply node that is configured to be coupled to a power supply, the circuit comprising: an isolating device coupled between the common power supply node and the power supply, the isolating device configured to connect the power supply to the common power supply node during a normal mode of operation of the pixel array, the isolating device configured to isolate the common power supply node from the power supply during a global mode of operation of the pixel array in combination with all other elements of the claim.

Regarding claims 5, and 18-20, the reason for allowance is as follows: the claims depend from allowable base claims.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian Jelinek whose telephone number is (571) 272-7366. The examiner can normally be reached on M-F 9:00 am - 5:00 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached at (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brian Jelinek
10/3/2005

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